TECHNIQUES FOR PATTERNING FEATURES IN SEMICONDUCTOR DEVICES

Field of the Invention

The present invention relates to semiconductor processing and, more particularly,
5   to reducing critical dimensions of features patterned in a semiconductor device.

Background of the Invention

Technology often demands the patterning of features smaller than those lithographically possible. For example, while patterning features, such as contact holes and vias, it may be desirable to have features with critical dimensions defined in the
10   substrate that are smaller than lithographically defined in the resist. The critical dimensions of a feature comprise the characteristic dimensions of the feature attained by the technology employed. Conventional techniques to reduce the critical dimensions of patterned features exist, however, these techniques have several drawbacks.

One common technique to reduce the critical dimensions includes the use of resist
15   reflow and overcoat films, e.g., resolution enhancement lithography assisted by chemical shrink (RELACS) processes. Resist reflow is extremely difficult to control because very small temperature variations across the bake plate can cause large variations in the critical dimensions across each wafer. Typical sensitivities are on the order of ten nanometers per degree celcius (nm/°C). Overcoat films can be spun on top of a photo-developed
20   chemically amplified resist. The photoacid from the resist diffuses into the overcoat film crosslinking it. The parts of the overcoat film that are not in physical contact with the resist, for example, a feature bottom, are not crosslinked, and therefore can be developed away. This technique, being highly specific to the resist type, is difficult to implement. Moreover, the crosslinked overcoat film offers poor etch resistance during the substrate
25   etch step, thus, negating any reductions in critical dimensions obtained. Silylating resists can also be used to chemically bias resist features, but they also suffer from cross-wafer

and nested-isolated bias issues. The above techniques may further result in features having corners that are not sharp, but rounded.

Another common technique is to use a polymerizing etch chemistry to induce a taper in the substrate thereby reducing the critical dimensions at a feature bottom. The critical dimensions of the feature at the top of the substrate are approximately the same as the critical dimensions obtained after etching an overlying layer, e.g., an antireflective layer. The feature sidewalls created in the substrate are slightly tapered, which is desirable for many applications. For example, after contact holes or vias are patterned in a dielectric layer, the copper seed layer deposition is facilitated by dielectric substrate sidewalls that are not perfectly vertical, but slightly tapered. However, the maximum amount of reduction of the critical dimensions depends on the amount of sidewall taper that can be tolerated. As an example, if the dielectric layer is about 500 nanometers (nm) thick and if the sidewall is about 88.5 degrees to the horizontal, the feature bottom will be approximately 20 nm smaller than the feature top. If the critical dimensions of the feature top is too large to begin with, the effectiveness of this technique is at best very limited.

Therefore, it would be desirable to have techniques for reducing the critical dimensions of patterned features that are effective, reproducible and versatile for patterning features having a broad range of critical dimension specifications. Further, techniques for reducing the critical dimensions of patterned features are needed that can be employed irrespective of the type of resist used, and provide for the mass-production of features that are uniform over entire wafers.

Summary of the Invention

The present invention provides techniques for semiconductor processing. In one aspect of the invention, a method for patterning one or more features in a semiconductor device comprises the following step. At least one critical dimension of the one or more features is reduced during etching of the antireflective material.

In another aspect of the invention, a lithographic structure comprises an antireflective material having a feature patterned therein, the feature having at least one reduced critical dimension.

A more complete understanding of the present invention, as well as further features and advantages of the present invention, will be obtained by reference to the following detailed description and drawings.

Brief Description of the Drawings

FIG. 1 is a diagram illustrating a semiconductor device with a feature having reduced critical dimensions etched therein using conventional techniques;

FIG. 2 is a diagram illustrating an exemplary technique for reducing the critical dimensions of a feature of a semiconductor device according to an embodiment of the present invention;

FIG. 3 is a collection of images illustrating the progressive patterning of a contact hole feature using silicon-containing antireflective material according to an embodiment of the present invention; and

FIG. 4 is a collection of images illustrating the progressive patterning of a contact hole feature using a tunable etch resistant antireflective material (TERA) according to an embodiment of the present invention.

Detailed Description of Preferred Embodiments

FIG. 1 is a diagram illustrating a semiconductor device with a feature having reduced critical dimensions etched therein using conventional techniques. As shown in FIG. 1, semiconductor device 100 comprises radiation sensitive imaging layer 102 deposited on antireflective material 104. Antireflective material 104 is deposited on substrate 106. Substrate 106 is deposited on nitride layer 108. Feature 110 is etched into radiation sensitive imaging layer 102, antireflective material 104 and substrate 106.

According to conventional methods for reducing the critical dimensions of etched features in semiconductor devices, the critical dimensions of feature 110 are changed, i.e., reduced, solely in substrate 106. As such, the critical dimensions of feature 110 remain unchanged during the etching of radiation sensitive imaging layer 102 and antireflective

5   material 104. Reduction of the critical dimensions of feature 110 in radiation sensitive imaging layer 102 or antireflective material 104 is practically impossible if either layer comprises predominately organic species, as is the case with semiconductor device 100.

As will be described below, the amount that the critical dimensions of a feature can be reduced, solely during etching of the substrate, is limited. Trying to reduce the

10   critical dimensions of a feature in a single layer, such as the substrate, may lead to artifacts that damage the feature.

FIG. 2 is a diagram illustrating an exemplary technique for reducing the critical dimensions of a feature of a semiconductor device. When processing semiconductor devices, the critical dimensions of a feature comprise the characteristic dimensions of the

15   feature attained by the technology employed. For example, when the feature comprises a contact hole, as is described in detail below, the critical dimensions may represent a measure of the diameter of the contact hole produced.

The techniques for reducing the critical dimensions of a feature may also be employed to tune the critical dimensions of the feature, as will be described in detail

20   below. The term "tune," as used herein, pertains to controlling the amount by which the critical dimensions are changed.

As shown in FIG. 2, semiconductor device 200 comprises radiation sensitive imaging layer 202 deposited on antireflective material 204. Antireflective material 204 is deposited on substrate 206. Substrate 206 is deposited on nitride layer 208. Feature 210

25   is etched into radiation sensitive imaging layer 202, antireflective material 204 and substrate 106, as is shown in steps 212, 214 and 216, respectively.

In step 212 of FIG. 2, feature 210 is etched into radiation sensitive imaging layer 202. During the etching of feature 210 into radiation sensitive imaging layer 202, the critical dimensions of feature 210 may change, or remain the same, as will be described in detail below. For example, the critical dimensions of feature 210 in step 212 of FIG. 2 do not change.

As will be further described below, radiation sensitive imaging layer 202 should be compositionally different from antireflective material 204, upon which radiation sensitive imaging layer 202 is deposited, to achieve a desired level of etch selectivity between the layers. Radiation sensitive imaging layer 202 may be deposited using any conventional deposition technique, including, but not limited to, spin on deposition and/or plasma enhanced chemical vapor deposition (PECVD).

Feature 210 may comprise any structure that may be introduced to a semiconductor device by lithographic techniques. Exemplary structures include, but are not limited to, contact holes, via patterns, lines, spaces, ovals and combinations comprising at least one of the foregoing features. As will be described in detail below, in conjunction with the description of FIGS. 3 and 4, an exemplary feature 210 comprises a contact hole.

As disclosed herein, the critical dimensions of feature 210 are reduced. For example, when feature 210 comprises a contact hole, the present techniques may be employed to reduce the diameter of the contact hole. When feature 210 comprises lines and spaces, the present techniques may be employed to reduce the spacing between lines.

In step 214 of FIG. 2, feature 210 is etched into antireflective material 204, which is deposited on substrate 206. Antireflective material 204 comprises one or more inorganic moieties. In an exemplary embodiment, antireflective material 204 has the structural formula M:C:H:X. The symbol 'M' represents a metallic element, including, but not limited to, silicon (Si), titanium (Ti), germanium (Ge), iron (Fe), boron (B), tin (Sn) and combinations comprising at least one of the foregoing metallic elements. The

symbol 'C' represents the element carbon. The symbol 'H' represents the element hydrogen. The symbol 'X' represents an inorganic element, including, but not limited to, oxygen (O), hydrogen, nitrogen (N) and combinations comprising at least one of the foregoing inorganic elements. In an exemplary embodiment, antireflective material 204 has the structural formula, Si:C:H:O.

Antireflective material 204 may be deposited on substrate 206 by any conventional deposition technique. In an exemplary embodiment, antireflective material 204 is deposited on substrate 206 using spin on processing. For example, when antireflective material 204 comprises silicon, antireflective material 204 may be deposited on substrate 206 by spin on processing. In another exemplary embodiment, antireflective material 204 is deposited on substrate 206 using PECVD. For example, antireflective material 204 may comprise a tunable etch resistant antireflective (TERA) coating comprising, for example, Si, C, O and H. When antireflective material 204 comprises a TERA coating, antireflective material 204 may be deposited on substrate 206 by PECVD. PECVD films tend to be conformal. Therefore, antireflective material 204 may comprise a conformally deposited material. Conformally deposited materials conform to the contours of the surface on which they are applied. When antireflective material 204 comprises a conformally deposited material, antireflective material 204 is typically deposited using PECVD.

The thickness of antireflective material 204 is dependent on the antireflective material composition. For example, when antireflective material 204 comprises silicon, and is deposited on substrate 206 using spin on processing, the thickness of antireflective material 204 may be greater than or equal to about 80 nanometers. In an exemplary embodiment, antireflective material 204 is deposited on substrate 206 using spin on processing to a thickness of about 80 nanometers, about 130 nanometers or greater than or equal to about 190 nanometers to optimize the antireflective properties.

The critical dimensions of feature 210 are reduced during the etching of antireflective material 204. Reducing, at least in part, the critical dimensions of feature 210 during the etching of antireflective material 204 is beneficial, as trying to completely reduce the critical dimensions of feature 210 solely during subsequent etching steps, i.e.,

5 during the etching of substrate 206, as described above in conjunction with the description of FIG. 1, if at all possible, may produce effects damaging to the feature. For example, trying to reduce of the critical dimensions of a feature solely during the etching of the substrate may lead to excessive tapering of the feature causing undesirable artifacts to occur, such as electrical shorting of adjacent features when, e.g., copper is plated.

10 To reduce the critical dimensions of feature 210 during etching of antireflective material 204, a plasma etching technique may be employed. The plasma etching technique comprises a plasma made up of gasses, including, but not limited to, fluorocarbon gas, argon gas, oxygen gas, nitrogen gas and combinations comprising at least one of the foregoing gasses. In an exemplary embodiment, plasma polymerizing

15 etch chemistries (hereinafter "plasma polymerizing etch") may be employed. The plasma polymerizing etch comprises at least one fluorocarbon gas, for example, C_4F_6, C_4F_8 and/or CH_3F as an etchant and as a polymeric species, nitrogen gas as a polymerization reaction aid which alters the plasma conditions, oxygen gas as a polymerization reaction control and argon gas as a source of argon ions which are needed to remove portions of the

20 fluoropolymer formed to prevent excessive amounts of polymerization and deposition. An exemplary plasma polymerizing etch, according to the teachings herein, comprises about 300 parts by volume argon gas, about 150 parts by volume nitrogen gas, about five parts by volume C_4F_8 gas, about five parts by volume oxygen gas and about five parts by volume CH_3F gas.

25 The plasma polymerizing etch deposits polymeric materials, typically in the form of layers (hereinafter "polymer layers"), on the walls of feature 210 during etching. The total thickness of the polymer layers deposited should be controlled such that the plasma

polymerizing etchant species may still diffuse through the polymer layers and etch antireflective material 204. The thickness of the polymer layers deposited depends on the composition of the polymeric materials and whether the particular surface is subject to ion bombardment. For example, during etching of feature 210, the thickness of the polymer layers deposited during etching of radiation sensitive imaging layer 202 is greater than the thickness of the polymer layers deposited during etching of antireflective material 204. In an exemplary embodiment, the total thickness of the polymer layers deposited during etching of radiation sensitive imaging layer 202 is up to about four nanometers at the thickest portion. For example, the total thickness of the polymer layers deposited during etching of radiation sensitive imaging layer 202 is between about one to about three nanometers at the thickest portion. The plasma polymerizing etch may be employed to reduce the critical dimensions of a feature by up to about 80 nanometers during etching of the antireflective material.

In step 214 of FIG. 2, the polymer layers deposited cause a reduction in the critical dimensions of feature 210 by causing the walls of feature 210 to taper in. The reduction, or 'choking', of feature 210 does not however require that the polymer layers deposited form such a gradually tapered configuration, so long as the polymer layers deposited reduce the critical dimensions of the feature.

In step 216 of FIG. 2, feature 210 is etched into substrate 206. Substrate 206 is deposited on nitride layer 208. Nitride layer 208 serves as a layer to stop the etching process. Nitride layer 208 comprises silicon nitride (Si_3N_4). Substrate 206 may comprise dielectric materials, including, but not limited to, oxide materials, such as fluorosilicate glass, borosilicate glass, borophosphorosilicate glass and combinations comprising at least one of the foregoing oxide materials. Substrate 206 may further comprise a low-k dielectric material. Suitable low-k dielectric materials include, but are not limited to, CORAL, a registered trademark of Novellus, SiLK a registered trademark of Dow

Chemical and FLARE a registered trademark of Honeywell, and combinations comprising at least one of the foregoing low-k dielectric materials.

Substrate 206 may be deposited on nitride layer 208 using any conventional deposition techniques. For example, when substrate 206 comprises CORAL, substrate 206 may be PECVD deposited. Further, when substrate 206 comprises SiLK and/or FLARE, substrate 206 may be deposited using spin on processing.

The critical dimensions of feature 210 may be further reduced during the etching of substrate 206. Plasma polymerizing etch may also be employed to reduce the critical dimensions of feature 210 in substrate 206 in a manner similar to that used to reduce the critical dimensions of feature 210 in antireflective material 204. The term 'Litho' and accompanying two-sided arrow are used to designate the critical dimensions of feature 210 created during lithography, and the term 'Etch' and accompanying two-sided arrow are used to designate the critical dimensions of feature 210 created during the etching process.

As was mentioned above, radiation sensitive imaging layer 202 is preferably compositionally different from antireflective material 204 to provide enhanced etch selectivity between the two layers. In an exemplary embodiment, radiation sensitive imaging layer 202 comprises organic moieties. Namely, radiation sensitive imaging layer 202 comprises primarily C, H, O and in some cases fluorine (F). Radiation sensitive imaging layer does not contain any metal atoms, such as Si atoms.

As mentioned above, the teachings presented herein may be used to tune the critical dimensions of a feature, e.g., control the amount by which the critical dimensions are changed. One exemplary technique for tuning the critical dimensions of a feature is by varying the amount of inorganic moieties present in the antireflective material. Namely, the greater the inorganic content of the antireflective material is, the greater the reduction in the critical dimensions will be. For example, the antireflective materials described herein may comprise up to about four atomic percent Si. However, the amount

of Si might be increased to attain a greater reduction in the critical dimensions of the feature. In an exemplary embodiment, the antireflective material comprises up to about ten atomic percent Si. In a further exemplary embodiment, the antireflective material comprises up to about 20 atomic percent Si.

5   Another exemplary technique for tuning the critical dimensions of a feature is by altering the composition of the plasma polymerizing etch employed to etch the antireflective material. As was mentioned above, an exemplary plasma polymerizing etch for etching the antireflective material comprises about 300 parts by volume argon gas, about 150 parts by volume nitrogen gas, about five parts by volume C_4F_8 gas, about five

10   parts by volume oxygen gas and about five parts by volume CH_3F gas. The composition may be altered to change the gas ratios therein. For example, the amount of C_4F_8 may be increased to about six parts by volume, and the amount of oxygen gas may be decreased to about four parts by volume to attain an increased reduction of the critical dimensions of the feature.

15   The flow of the plasma polymerizing etch may also be altered to tune the critical dimensions of a feature. Namely, nitrogen gas flows are generally much larger than fluorocarbon and oxygen gas flows. Whereas the flow of the exemplary plasma polymerizing etch highlighted above would be at about 50 standard cubic centimeters per minute (sccm), altering the nitrogen gas content could increase the flow up to about 300

20   sccm.

FIG. 3 shows the etching of a feature in a semiconductor device according to the techniques presented herein. As shown in FIG. 3, semiconductor device 300 comprises radiation sensitive imaging layer 202 deposited on antireflective material 204. Antireflective material 204 is deposited on substrate 206. Feature 210 is etched into

25   radiation sensitive imaging layer 202, antireflective material 204 and substrate 206.

Specifically, FIG. 3 is a collection of images illustrating the progressive patterning of a contact hole feature using a silicon-containing antireflective material. In step 302 of

FIG. 3, feature 210, i.e., a contact hole, is etched into radiation sensitive imaging layer 202. The critical dimensions of feature 210 are not changed during etching of radiation sensitive imaging layer 202. Radiation sensitive imaging layer 202 is formed over antireflective material 204.

5   In step 304 of FIG. 3, feature 210 is further etched into antireflective material 204. The critical dimensions of feature 210 are reduced by tapering through antireflective material 204. In step 306 of FIG. 3, feature 210 is further etched into substrate 206. The critical dimensions of feature 210 are further reduced by tapering through substrate 206.

Similarly, FIG. 4 also shows the etching of a feature in a semiconductor device

10   according to the techniques presented herein. As shown in FIG. 4, semiconductor device 400 comprises radiation sensitive imaging layer 202 deposited on antireflective material 204. Antireflective material 204 is deposited on substrate 206. Feature 210 is etched into radiation sensitive imaging layer 202, antireflective material 204 and substrate 206.

Specifically, FIG. 4 is a collection of images illustrating the progressive patterning

15   of a contact hole feature using a tunable etch resistant antireflective material (TERA). In step 402 of FIG. 4, feature 210 is etched into radiation sensitive imaging layer 202. The critical dimensions of feature 210 are not changed during the etching of radiation sensitive imaging layer 202. Namely, the diameter of the contact hole remains at approximately 140 nanometers throughout radiation sensitive imaging layer 202. In step

20   404 of FIG. 4, feature 210 is further etched into antireflective material 204 and substrate 206. The critical dimensions of feature 210 are reduced by about 40 nanometers during the etching of antireflective material 204 and during the etching of substrate 206.

Thus, the inventive technique described herein results in the generation of an improved lithographic structure. The lithographic structure may comprise a substrate, an

25   antireflective material over the substrate and a radiation sensitive imaging layer over the antireflective material. The antireflective material has a feature patterned therein. The

feature has reduced critical dimensions. Further, the substrate may have a feature patterned therein. The feature may also have reduced critical dimensions.

Although illustrative embodiments of the present invention have been described herein, it is to be understood that the invention is not limited to those precise embodiments, and that various other changes and modifications may be made by one skilled in the art without departing from the scope or spirit of the invention.